## Remarks

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks. Claims 1-23 are pending in the application. Claims 1-23 are rejected. No claims have been allowed. Claims 1, 13, 18, and 21 are independent. Claims 1, 8-11, 13, 15, 16, 20, 21 and 23 have been amended.

### *Cited Art*

The Action cites:

U.S. Patent No. 7,003,753 (hereinafter "Teene");

U.S. Publication No. 2004/0083437 (hereinafter "Gullapalli"); and

U.S. Patent No. 6,530,065 (hereinafter "McDonald").

### *Claim Rejections under 35 U.S.C. § 101*

The Action rejects claims 13-17 and 21-23 under 35 U.S.C. § 101 as allegedly directed toward non-statutory subject matter. Applicants respectfully traverse these rejections. Independent claim 13 has been amended to recite "An analog or RF simulator of a computer for simulating a circuit…" and independent claim 21 has been amended to recite "using a computer, generating a system of equations…." Thus, claims 13-17 and 21-23 are directed to statutory subject matter and these rejections should be withdrawn. Exemplary support for these amendments can be found in the specification at page 1, lines 18-19; page 5, lines 5-21; and page 10, lines 13-27.

### *Claim Rejections under 35 U.S.C. § 112*

The Action rejects claims 18-20 under 35 USC § 112, first paragraph. Applicants respectfully traverse these rejections.

The instant specification and figures contain sufficiently detailed description of structure to support the functions recited in claims 18-20. For example, the "means for reading" language of independent claim 18 can be implemented by the analog or RF simulator 12, which comprises "an elaboration engine 14 coupled to a simulator kernel 16. The simulator kernel 16 includes one or both of a direct solver 18 and a linear iterative solver 20." (Specification, page 5, lines 6-7 and Fig. 1.) The specification states "the simulator 12 reads the netlist that includes a

circuit description containing both components and parasitic information." (Specification, page 5, lines 22-24.)

The "means for generating" language of claim 18 is also sufficiently supported in the specification. For example, the simulator 12 can implement the "generating" function. Fig. 2 is a flow chart of a method for performing the simulation of a circuit using the simulator 12. (Specification, page 5, lines 22-23.) In block 42 of Fig. 2, the simulator 12 defines two circuit descriptions to be used in the simulation. (Specification, page 5, lines 26-28.) Fig. 3 shows a more detailed flowchart of block 42 of Fig. 2. (Specification, page 6, line 19.) In block 70 of Fig. 3, the simulator removes parasitic information from a first circuit description to create a second circuit description without the parasitic information. (Specification, page 7, lines 7-9.)

The "means for simulating" language of claim 18 is also sufficiently supported in the specification. For example, the simulator 12 can implement the "simulating" function using elaboration engine 14 and simulation kernel 16. In block 44 of Fig. 2 and in Fig. 4, the simulator 12 simulates a circuit using both a circuit description comprising parasitic information and a circuit description with reduced parasitic information. (Specification, page 8, lines 7-23.)

The "means for solving" language of claim 19 is also sufficiently supported in the specification. For example, the simulator kernel 16 of the simulator 12 can implement the "solving" function. "The simulation kernel includes one or both of a direct solver 18 and a linear solver 20. Generally, the simulation kernel forms a system of linear equations or non-linear equations to solve the well-known circuit equations Ax=B or F(x)=0, respectively." (Specification, page 5, lines 7-11.) Figs. 6 and 7 and the correspond description on pages 9 and 10 of the specification describe in detail how the simulation kernel 16 solves these equations.

The Action rejects claims 8-10, 15, 16, 18-20 and 23 under 35 USC § 112, second paragraph. Applicants respectfully traverse these rejections.

Claim 8 has been amended to recite "evaluating $F(X^i)$, where F is a function and $X^i$ is a value of a variable X for an iteration *i*," such that the symbols of the mathematical notation are sufficiently described. See page 9, lines 1-23 for exemplary support for this amendment. The § 112 rejection of claim 8 should therefore be withdrawn.

Claim 9 has been amended to recite "J is a Jacobian matrix related to the circuit components and built using the second circuit description, $\Delta X$ is a variable to be solved, F is a function, and $X^i$ is a value of a variable X for an iteration *i*; factorizing the matrix J; evaluating

$F(X^i)$ using the first circuit description; and solving for $\Delta X$." Claim 9, as amended, recites a single definition of J. Furthermore, the relationship of $F(X^i)$ and the first circuit description is clear: simulating the circuit comprises evaluating $F(X^i)$ using the first circuit description. The § 112 rejection of claim 9 should therefore be withdrawn.

Claim 10 has been amended to recite "The method of claim 1, further comprising any one or more of the following: DC, AC, transient analysis, state-state analysis and modulated steady-state analysis." Claim 10, as amended, recites a further limitation to the method of claim 1. The § 112 rejection of claim 10 should therefore be withdrawn.

Claim 15 has been amended to recite "the one or more lists include a netlist and a file comprising parasitic information." The § 112 rejection of claim 15 should therefore be withdrawn.

Claim 16 has been amended to recite "the simulation kernel evaluates $F(X^i)$, where F is a function and $X^i$ is a value of a variable X for an iteration *i*," such that the symbols of the mathematical notation are sufficiently described. The § 112 rejection of claim 16 should therefore be withdrawn.

Regarding claims 18-20, Applicants submit that the specification and figures contain sufficiently detailed description of structure to implement the functions recited in claim 18-20, as discussed in detail above. These § 112 rejections of claims 18-20 should therefore be withdrawn.

Claim 20 has been amended to recite "the means for simulating is capable of evaluating $F(X^i)$, where F is a function and $X^i$ is a value of a variable X for an iteration *i* ...." The symbols of the mathematical notation are sufficiently described. Claim 20, as amended, does not recite a method language to limit the simulator of claim 18. Amended claim 20 further clarifies that the matrix J is built using the second circuit description. This § 112 rejection of claim 20 should therefore be withdrawn.

Claim 23 has been amended to recite "solving further comprises factorizing the Jacobian matrix J, which is built using the second circuit description, evaluating $F(X^i)$ using the second circuit description, and solving for $\Delta X$." The second circuit description is defined in claim 21. The § 112 rejection of claim 23 should therefore be withdrawn.

***Claim Rejections under 35 U.S.C. § 102***

The Action rejects claims 1-3, 7, and 10 under 35 U.S.C. 102(e) as being anticipated by Teene. Applicants respectfully traverse these rejections.

Independent claim 1 is not anticipated by Teene at least because Teene does not teach each and every element of claim 1. Claim 1, as amended, requires two different circuit descriptions and simulating using both circuit descriptions in order to generate a single simulation result. Figure 1 shows an example of two circuit descriptions at 22 and 24. Notably, both circuit descriptions are input into the simulator 12 to obtain single simulation results 30.

Teene mentions a "functional simulation" that "generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation" (3:60-63) and a "full instance resistance and capacitance extraction" in which "a layout extraction is performed to determine the values of all the parasitic capacitances and resistances" (4:10-19). Teene clearly does not teach or even suggest using two different circuit descriptions in a single simulation, as required by amended claim 1. To the contrary, Teene seems to teach not using either the functional simulation, because of the lack of accuracy, or the full instance extraction, because it is too "computer-intensive" and "time-consuming" (4:16-19).

Because Teene does not teach or suggest each and every element of amended claim 1, claim 1 is allowable over Teene. Claims 2, 3, 7 and 10 depend from claim 1 and are thus allowable for the same reasons as claim 1, and because each dependent claim recites a distinctly patentable combination of features.

***Claim Rejections under 35 U.S.C. § 103***

The Action rejects claims 4, 5 and 18 under 35 U.S.C § 103(a) as unpatentable over Teene. Applicants respectfully traverse these rejections.

Claims 4 and 5 depend from claim 1 and are not obvious over Teene at least because Teene does not teach or suggest each and every element of claim 1. For example, Teene does not teach or suggest "simulating the circuit using both the first and second circuit descriptions" as discussed above. To the contrary, Teene suggest not using either the "function simulation" approach, due to the lack of accuracy, or the "full instance" approach, due to the extreme amount time and computer resources required. Because claims 4 and 5 are not obvious over Teene, the rejections of claims 4 and 5 should be withdrawn.

Independent claim 18 is not obvious over Teene at least because Teene does not teach or suggest each and every element of claim 18. For example, Teene does not teach or suggest "means for simulating the circuit using substantially the first circuit description comprising the parasitic information and the second circuit description with reduced parasitic information" as recited in independent claim 18. The Action cites column 4, lines 10-14, of Teene in reference to this element of claim 18. However, this paragraph of Teene only describes the "full instance" approach to simulating a circuit. Neither this paragraph, nor any other portion of Teene, teaches or suggests means for simulating a circuit using two different circuit descriptions.

Because Teene does not teach or suggest every element of claim 18, claim 18 is not obvious over Teene. The rejection of claim 18 should therefore be withdrawn.

The Action rejects claims 6, 8, 9, 11, 13-16, and 19-23 under 35 U.S.C § 103(a) as unpatentable over Teene in view of Gullapalli. Applicants respectfully traverse these rejections.

Claims 6, 8, 9 and 11 depend from independent claim 1 and are allowable over Teene for the same reasons a claim 1. Claims 19 and 20 depend from independent claim 18 and are allowable over Teene for the same reasons as claim 18. The addition of Gullapalli does not cure the deficiencies of Teene with respect to independent claims 1 and 18. For example, Gullapalli does not teach or suggest simulating a circuit using two different circuit descriptions. Therefore, dependent claims 6, 8, 9, 11, 19 and 20 are allowable over Teene in view of Gullapalli and the rejection of these claims should be withdrawn.

Independent claim 13, as amended, is not obvious over the combination of Teene and Gullapalli at least because the combination does not teach or suggest "an elaboration engine … that defines a first circuit description used for accuracy of the simulation and a second circuit description used for speed of the simulation, the first circuit description being different from the second circuit description" as recited in amended independent claim 13.

Teene teaches in column 3 a "functional" simulation of a circuit that does not include all the parasitic information of the circuit. Teene teaches in column 4 a "full instance" simulation of a circuit that does include all the parasitic information of the circuit. However, Teene does not teach or suggest a single "elaboration engine" that defines both of these circuit simulations. Teene describes two different flow diagrams 400, 500 representing two unrelated approaches to simulating a circuit.

Gullapalli also fails to teach an elaboration engine that defines the two different circuit descriptions recited in amended claim 13. Gullapalli teaches only a single circuit description. "In block 12, a circuit description and corresponding circuit elements are provided." (Gullapalli, ¶0009.)

Because the combination of Teene and Gullapalli does not teach or suggest every element of amended independent claim 13, claim 13 and its depended claims 14-16 are allowable over these Teene and Gullapalli. The rejections of claims 13-16 should therefore be withdrawn.

Independent claim 21 is not obvious over the combination of Teene and Gullapalli at least because the combination does not teach or suggest "generating a system of equations wherein a part of the system of equations uses a first circuit description comprising parasitic information and a part of the system of equations uses a second circuit description with parasitic information removed" as recited in claim 21.

The Action alleges that Gullapalli teaches this feature of claim 21 at paragraphs 0021-0022. (Action, page 23.) However, this language of Gullapalli does not mention anything about generating a system of equations that uses two different circuit descriptions. By contrast, Gullapalli relies on a single circuit description to generate circuit equations. "In block 14, circuit equations are generated based on *the* circuit description and models." (Gullapalli, ¶0010.)

Teene also does not teach or suggest generating a system of equations that uses two different circuit descriptions. Instead, Teene teaches "receiving as an input a representation of a core cell for a hierarchical integrated circuit design" and "generating a physical netlist for a core cell model tile that maps logical ports of the core cell to physical ports of the core cell model tile." (Teene, column 5, lines 4-8.)

Because the combination of Teene and Gullapalli does not teach or suggest every element of amended independent claim 21, claim 21 and its depended claims 22 and 23 are allowable over these Teene and Gullapalli. The rejections of claims 21-23 should therefore be withdrawn.

The Action rejects claim 12 under 35 U.S.C § 103(a) as unpatentable over Teene in view of McDonald. Applicants respectfully traverse this rejection. Claim 12 depends from independent claim 1 and is allowable over Teene for the same reasons a claim 1. The addition of McDonald does not cure the deficiencies of Teene with respect to independent claim 1. For example, McDonald does not teach or suggest simulating a circuit using two different circuit

descriptions, as recited in claim 1. Therefore, dependent claim 12 is allowable over Teene in view of McDonald and the rejection of claim 12 should be withdrawn.

The Action rejects claim 17 under 35 U.S.C § 103(a) as unpatentable over Teene in view of Gullapalli and further in view of McDonald. Applicants respectfully traverse this rejection. Claim 17 depends from independent claim 13 and is allowable over Teene and Gullapalli for the same reasons a claim 13. The addition of McDonald does not cure the deficiencies of Teene and McDonald with respect to independent claim 13. For example, McDonald does not teach or suggest an elaboration engine that defines the two different circuit descriptions. Therefore, dependent claim 17 is allowable over Teene and Gullapalli in view of McDonald and the rejection of claim 17 should be withdrawn.

***Interview Request***

If the claims are not found by the Examiner to be allowable, the Examiner is requested to call the undersigned attorney to set up an interview to discuss this application.

***Conclusion***

The claims in their present form should be allowable. Such action is respectfully requested.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

One World Trade Center, Suite 1600
121 S.W. Salmon Street
Portland, Oregon 97204
Telephone: (503) 595-5300
Facsimile: (503) 595-5301

By /Sandon M. Duncan/
Sandon M. Duncan
Registration No. 64,141